Caracteristiques SPARTAN 6 XILINX LX45

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General

- consommation: 0.6A
- 45nm low power process technology with 6-input LUTs
- 1080MHz clock management tiles (2 DCM + 1 PLL)
- 320MHz Block RAM from 216 - 4824 Kbits
- Memory interface controllers blocks from 0 - 4
- 1.08Gbps SelectIO™ technology
- 390MHz DSP48A1 slices from 8 - 180
- Embedded processing

Spartan-6 Family:

- Spartan-6 LX FPGA: Logic optimized [✔]
- Spartan-6 LXT FPGA: High-speed serial connectivity [✘]

Designed for low cost

- Multiple efficient integrated blocks
- Optimized selection of I/O standards
- Staggered pads
- High-volume plastic wire-bonded packages

Low static and dynamic power

- 45 nm process optimized for cost and low power
- Hibernate power-down mode for zero power
- Suspend mode maintains state and configuration with multi-pin wake-up, control enhancement
- Lower-power 1.0V core voltage (LX FPGAs, -1L only) [✔]
- High performance 1.2V core voltage (LX and LXT FPGAs, -2, -3, and -3N speed grades)

Multi-voltage, multi-standard SelectIO™ interface banks

- Up to 1,080 Mb/s data transfer rate per differential I/O
- Selectable output drive, up to 24 mA per pin
- 3.3V to 1.2V I/O standards and protocols
- Low-cost HSTL and SSTL memory interfaces
- Hot swap compliance
- Adjustable I/O slew rates to improve signal integrity

High-speed GTP serial transceivers in the LXT FPGAs[✘]

- Up to 3.2 Gb/s
- High-speed interfaces including: Serial ATA, Aurora, 1G Ethernet, PCI Express, OBSAI, CPRI, EPON, GPON, DisplayPort, and XAUI

Integrated Endpoint block for PCI Express designs (LXT) [✘]

Low-cost PCI® technology support compatible with the 33 MHz, 32- and 64-bit specification.
Efficient DSP48A1 slices

- High-performance arithmetic and signal processing
- Fast 18 x 18 multiplier and 48-bit accumulator
- Pipelining and cascading capability
- Pre-adder to assist filter applications

Integrated Memory Controller blocks

- DDR, DDR2, DDR3, and LPDDR support
- Data rates up to 800 Mb/s (12.8 Gb/s peak bandwidth)
- Multi-port bus structure with independent FIFO to reduce design timing issues

Abundant logic resources with increased logic capacity

- Optional shift register or distributed RAM support
- Efficient 6-input LUTs improve performance and minimize power
- LUT with dual flip-flops for pipeline centric applications

Block RAM with a wide range of granularity

- Fast block RAM with byte write enable
- 18 Kb blocks that can be optionally programmed as two independent 9 Kb block RAMs

Clock Management Tile (CMT) for enhanced performance

- Low noise, flexible clocking
- Digital Clock Managers (DCMs) eliminate clock skew and duty cycle distortion
- Phase-Locked Loops (PLLs) for low-jitter clocking
- Frequency synthesis with simultaneous multiplication, division, and phase shifting
- Sixteen low-skew global clock networks

Simplified configuration, supports low-cost standards

- 2-pin auto-detect configuration
- Broad third-party SPI (up to x4) and NOR flash support
- Feature rich Xilinx Platform Flash with JTAG
- MultiBoot support for remote upgrade with multiple bitstreams, using watchdog protection

Enhanced security for design protection

- Unique Device DNA identifier for design authentication
- AES bitstream encryption in the larger devices